Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-2, 4, 6-25, 49-64 and 66-70 (Canceled).

71. (Previously Presented) An integrated circuit package comprising:

a silicon die having a first thickness;

a substrate having a first side and a second side;

a transition medium disposed between the silicon die and the first side of the substrate; and

a mold cap which encapsulates the silicon die and the transition medium, wherein the transition medium and the mold cap expand and contract at approximately the same rate in response to temperature changes so as to reduce thermal stress on the silicon die during thermal cycling.

72. (Previously Presented) The integrated circuit package of claim 71, wherein the transition medium and the mold cap have approximately equal coefficients of thermal expansion.

73. (Previously Presented) The integrated circuit package of claim 71, wherein the mold cap and transition medium have coefficients of thermal expansion between approximately $7 \times 10^{-6}/^{o}C$ and $15 \times 10^{-6}/^{o}C$.

74. (Previously Presented) The integrated circuit package of claim 71, wherein the transition medium has a second thickness, and the first thickness of the silicon die is less than the second thickness of the transition medium.

75. (Previously Presented) The integrated circuit package of claim 71, wherein a first edge of the transition medium is coincident with a first edge of the silicon die, and a second edge of the transition medium is coincident with a second edge of the silicon die.

76. (Previously Presented) The integrated circuit package of claim 71 wherein a thickness of the substrate and a thickness of the mold cap define a package thickness, wherein the silicon die is disposed at a location approximately equally spaced from the bottom of the substrate and the top of the mold cap.

77. (Previously Presented) The integrated circuit package of claim 76 wherein the mold cap has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the transition medium such that the die remains relatively motionless within the integrated circuit package during thermal cycling.

78. (Previously Presented) The integrated circuit package of claim 71 wherein the silicon die is coupled to the transition medium through an adhesive.

79. (Previously Presented) The integrated circuit package of claim 78, wherein a coefficient of thermal expansion for the adhesive is approximately 58 x 10^{-6}/°C.

80. (Previously Presented) The integrated circuit package of claim 71 wherein the substrate is a tape carrier having a dielectric layer and a conductive layer.

81. (Previously Presented) The integrated circuit package of claim 80 comprising solder balls mounted to the second side of the substrate, the solder balls electrically contacting an etched circuit in a conductive layer of the tape carrier and adapted to electrically connect the integrated circuit package to a printed circuit board.

82. (Previously Presented) The integrated circuit package of claim 81, wherein the transition medium and the mold cap have coefficients of thermal expansion less than a coefficient of thermal expansion of the printed circuit board to which the integrated circuit

package is capable of being coupled with and greater than a coefficient of thermal expansion of the silicon die.

83. (Previously Presented) An integrated circuit package comprising:

a silicon die having a first thickness;

a metallized polymer layer having a first side and a second side;

a transition medium having a second thickness and disposed between the silicon die and the first side of the metallized polymer layer; and

a mold cap which encapsulates the silicon die and the transition medium, wherein the mold cap and transition medium expand and contract in response to temperature changes such that the die remains relatively motionless within the integrated circuit package during thermal cycling.

84. (Previously Presented) The integrated circuit package of claim 83, wherein the mold cap defines a third thickness and the metallized polymer layer defines a fourth thickness, wherein the third thickness and fourth thickness define a package thickness, and wherein the silicon die is disposed near the middle of the package thickness so as to reduce warping of the integrated circuit package in response to thermal expansion of the die.

85. (Previously Presented) The integrated circuit package of claim 83, wherein the first thickness is less than the second thickness.

86. (Previously Presented) The integrated circuit package of claim 83, wherein the mold cap and the transition medium each comprise a first mold compound, such that coefficients of thermal expansion of the transition medium and mold cap are approximately equal.

87. (Previously Presented) The integrated circuit package of claim 83, wherein the mold cap and transition medium have coefficients of thermal expansion between approximately 7 x 10^{-6}/°C and 15 x 10^{-6}/°C.

88. (Previously Presented) The integrated circuit package of claim 83, wherein a first edge of the transition medium is coincident with a first edge of the silicon die, and a second edge of the transition medium is coincident with a second edge of the silicon die.

89. (Previously Presented) The integrated circuit of claim 83, wherein the metallized polymer layer is a tape carrier comprising solder balls mounted to the second side of the metallized polymer layer, the solder balls electrically contacting an etched circuit in a conductive layer of the tape carrier and adapted to electrically connect the integrated circuit package to a printed circuit board.

90. (Previously Presented) The integrated circuit of claim 89, wherein the transition medium and the mold cap have coefficients of thermal expansion less than a coefficient of thermal expansion of the printed circuit board to which the integrated circuit package is capable of being coupled with and greater than a coefficient of thermal expansion of the silicon die.